International Journal On Engineering Technology and Sciences – IJETS™
ISSN(P):2349-3968,ISSN(O):2349-3976
Volume X, Issue IX, September - 2023

DESIGN AND ANALYSIS OF CNTFET FULL ADDER USING XOR LOGIC

[1]A.Gangadevi , [2]K.Sumathi,
[1]PG Scholar, [2]Professor, [1,2]Department of Electronics and Communication Engineering, Akshaya College of Engineering and Technology.
gangadevia08@gmail.com, sumathik@acetcbe.edu.in

Abstract-- *As the scaling process advances, interest in carbon nanotube field effect transistors is growing. They might offer a solution to the difficulties associated with scaling the CMOS art. The design and analysis of a complete adder that employs xor logic will be covered in this article. We'll also look at how to use a neural network to digitally rewire a biquadratic multifunctional filter that use a single 32 nm CNTFET-based DCC node to build digital logic circuits. The design makes use of a single DVCC block built on a CNTFET as well as a sparse arrangement of capacitors and resistors. This digitally reconfigurable multi-functional filter circuit can use a similar topology to provide programmable low-pass, high-pass, and band-pass filter combinations.*

Keywords: Carbon Nano Tune, CNTFET, CMOS, Logic Circuits, Artificial Neural Network

Introduction

Low power consumption in integrated circuits is important, as evidenced by the rise of mobile, laptop, and tablet devices. Power consumption may decrease when the number of transistors decreases. Complementary MOS (Metal Oxide Semiconductor) CMOS technology has played a crucial role in the advancement of the fields of computing, telecommunications, and electronics during the past few decades. Increased speed, less power dissipation, lower prices, and more integration density are all made possible by shrinking the size of the core component. Because of their better qualities, carbon nanotube (CNT) field effect transistors have been proposed as a viable replacement for CMOS devices. The outstanding performance of CMOS transistors is nonetheless hindered by process modifications, random variances, and leakage currents as the size of CMOS transistors continues to drop. The carbon nano tube field effect transistor or CNFET has also been mentioned as one of the possible candidates to provide a platform for next generation electronic devices. A CNFET, a molecular device, features three terminals: the gate, the source, and the drain. The CNFET uses a semiconductor carbon nano tube, or CNT, as a channel to establish a connection between the sources and drain electrodes. In the post-silicon age, CNFETs are being investigated as prospective options because of their exceptional Electrical and structural characteristics, as shown in Figure 1. They have many benefits, including as improved mobility, enhanced carrying capacity, higher transconductance, reduced intrinsic capacitance, and a higher subthreshold gradient. These features point to a potential that exceeds silicon nanoelectronics and notably show greater performance compared to conventional CMOS models, especially in the switching scenario. Additionally, a lot of research has been done on CNCFETs due to their high transverse conductivity.

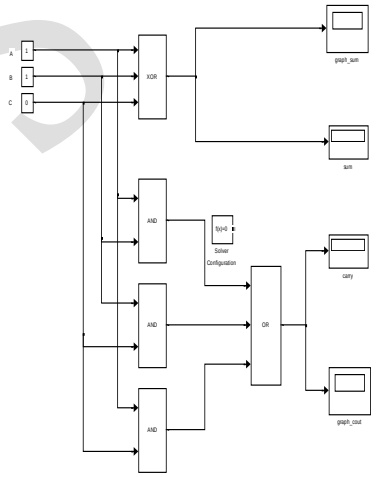

Figure.1 Full Adder

A proposed design and redesigned version of the Single Input Multi Outfit Voltage Mode Multi-functional proposed circuit, which has been optimized with CNFETs and is digitally controlled with summing network, have been used in this paper to develop a CNFET-based design to create a highly efficient and low power adder. Additionally, all of these designs rely on modifying the tube diameter to change the threshold voltage, which requires a difficult and expensive fabrication method in addition to a number of advancements over the present CMOS transistor technology. It is a very helpful building component that may be used to create many voltage and current-mode circuits, including amplifiers, oscillators,

and even multi-function filters. The analog signal processing circuit known as the DVCC uses differential inputs and is PDP amongst the most advanced designs, we have addressed these issues in this work using the same diameters and threshold voltages for all devices as well as drawing post layout for each design based on the customized industrial fabrication process.

II-Carbon Nano Tube Field Effect Transistor

Cobalt Nanotube Graphite sheets are rolled into cylindrical tubes to form CNTs. The metallic or semiconductor chirality vector of CNTs can be either (a,b) dependent on the values of CNTs. You can tell if a substance is metallic or semiconductor in nature by looking at the chirality vector of single wall SWCNTs and multi wall MWCNTs. Carbon nanotube fields are used as the channel by a particular class of transistor known as CNTs. The two different types of CNTs are MOSFET-like CNTFETs and Schottky Barrier Network Transistors (SBCN TFET). The advantage of CNTFET over CMOS is its ability to control the threshold voltage, which is determinable using equation. $V_t = \frac{0.43}{d_{cnt}}$

$$S = x \oplus y \oplus z$$

$$S = (\overline{z \oplus y})^2 z + (\overline{x \oplus y})\bar{z}$$

$$S = \bar{k}z + k\bar{z}$$

$$cout = xy + xz + yz$$

$$cout = \overline{x \oplus y}\, x + (x \oplus y)z$$

$$cout = \bar{k}.x + kz$$

$$d_{cnt} = \frac{0.249\sqrt{{a_1}^2 + {b_1}^2 + a_1 b_1}}{\pi}$$

Here, Carbon to carbon atom distance is 0.249nm. To reduce static power consumption and delay, it requires a high number of transistors, which in turn increases power consumption. Therefore, to achieve full-swing outputs with minimum transistor count, the highest performance, and the lowest static power Table1.a and 1b consumption, a method has been applied to all three, sum S, cout, module are verified, Therefore, we used x and x_ as common intermediate signals to Implement sum and cout modules using the proposed method:

Switch Control	In1	In2	cout	Switch Control	In1	In2	cout
k=0	a=1		1	k=0	$\bar{a}$=0		vdd
k=1		c=1	1	K =0		$\bar{c}$=0	vdd
k=1		c=0	0	k=1		$\bar{c}$=1	gnd
k=0	a=0		0	K =1	$\bar{a}$=1		gnd

This method of multiplexer design is based on the design of pass transistor multiplexers. Table 1a illustrates the truth table for the cout module multiplexer, where h is the switch control, and x and z are the inputs and cout is the output. Each input is capable of having two states, thus allowing for four outputs, of which two are logical 1 and another one is logical 0. In order to have a full-swing output, two rules must be followed to, for a logic 1 output, P-doped tubes must be designed in a series, with all triggering signals (switch control and inputs) being logic 0. For a logic 0 output, an N-doped tube design must be designed with all triggering signals being logic 1. Logic 0 is input in the first 2 rows, and logic 1 is input in the last 2 rows. We can see that Table 1b is created by inverting these two signals. The outcome of this exercise is Table 1c which illustrates the selected signals and the logic to be applied to the cout module design. In this table, those with direct voltage drain drain VDD- and ground GND-connections are implemented directly and are capable of amplifying the input signals; those without a direct VDD- or GND-connection are designed using a complement of inputs (1) and (2) as VDD-and GND connections. The newer designs utilise less space compared to the previous iteration. However, they incur a high delay when used in a carry propagation path. Consequently, in the suggested circuits, the cout module has been developed using VDD connections and GND connections.

III - MULTIPLE-FUNCTIONAL FILTER

Figure 3 illustrates the circuit of a voltage mode multiple-function filter utilizing CMOS technology, which has been re-engineered as a digital reconfigurable nano-tubular filter

International Journal On Engineering Technology and Sciences – IJETS™
ISSN(P):2349-3968,ISSN(O):2349-3976
Volume X, Issue IX, September - 2023

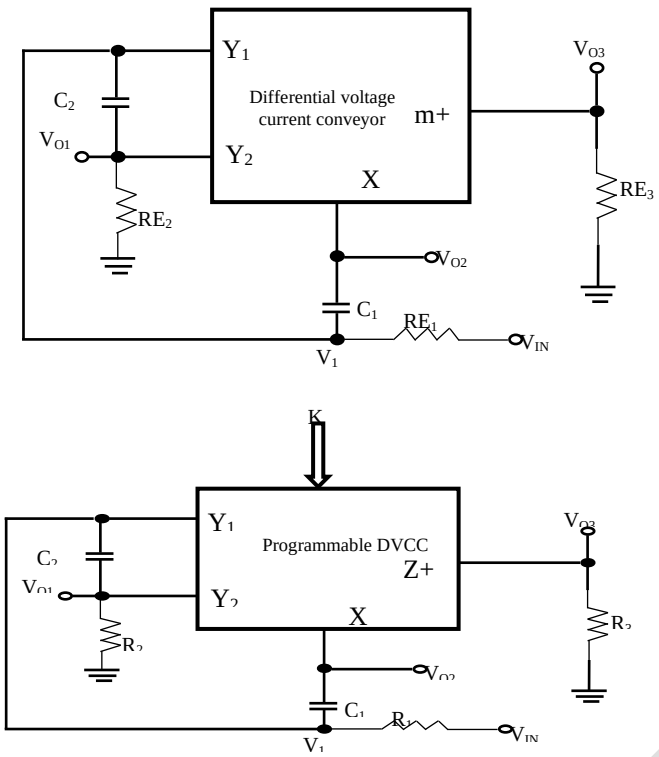

Figure. 2a and 2b Filter Circuit

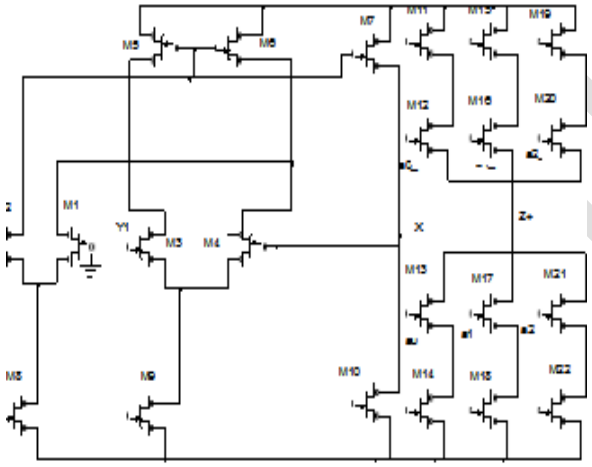

Figure.3. Optimized Transistors Technology

The number of CNTs, Inter-Cnt Pitch, and diameter of the CNTs (DCNTs) have been selected with the aim of achieving optimal differential voltage current conveyor DVCC performance as shown in Figure. 2a. subsequently, the circuit was digitally programmable with the use of the current summing network technology. The configured circuit provides the band pass, low pass, and high pass filters as shown in Figure.3.

$$BB_S = \frac{sC_2RE_1}{s^2C_1C_2 + sRE_2(RE_1 + RE_2) + RE_1RE_2}$$

$$L_{PS} = \frac{RE_1RE_2}{s^2C_1C_2 + sRE_2(RE_1 + RE_2) + RE_1RE_2}$$

$$H_{PP} = \frac{-G_1}{G_3}\frac{s^2C_1C_2}{s^2C_1C_2 + sRE_2(RE_1 + RE_2) + RE_1RE_2}$$

$$RE_1 = \frac{1}{RE_1}, RE_2 = \frac{1}{RE_2}, RE_3 = \frac{1}{RE_3}$$

This circuit takes care of all the filters, like the Biquadratic Band Pass (BBS), Low Pass (LPS), and High Pass (HPP) filters, all at the same time, without having to change the values of any of the passive components. We're simulating the DVCC Multifunctional filter at a supply voltage of VDD 0.9V with a thirty-two nm.

The circuit is re-arranged for f (1.06), q (0.5) depending on the resistance RE1, RE2, RE3, 15kΩ, capacitance C1, C2, 15 femtofarad. The frequency of the proposed filter could be improved by adjusting the CNFET optimized parameters, especially DCNT Diameter, but at the expense of decreased power dissipation.

The matrix determines the terminal properties of the reconfigurable DC current conveyor. Programmable DVCCs are used to demonstrate the factor of reconfigurability in the DVCC multi-layered filter as shown in Figure. 2b. The Digital control word (DCL) is created by the addition of SN (Current Summing Network) at m+ terminal, which is expressed as a value between 1 and 2n-1, where n is the number of transistors arrayed simultaneously. SN is used to regulate the present transfer gain parameter. The current flow out of the m+ terminal of programmable DVCC is indicated and the present transfer gain parameter is determined, where di represents the digital code bits applied to the nth branch of CSN. The current flow in the specified branch is either allowed or prohibited depending on the value of logic 1, or logic 0, respectively.

The CNFET transistors of programmable DVCC have been individually optimized in terms of design parameters i.e. Number of CNT's, Inter-CNT Pitch and Diameter of CNT to obtain an improved high frequency response. While designing, it has been ensured that the inherent port characteristics of the DVCC reflect near to ideal behaviour.

IV - OPTIMIZED FILTER

The programmable digital frequency conversion circuit (DFC) has been developed and is now used as the fundamental component for a programmable multifunctional filter. Figure 3b illustrates the proposed

circuit of a programmable-DFC multifunctional Filter utilizing CNFET Technology, which includes a tunability factor based on the current summing net. This circuit not only realizes the filter function of Low-Pass, High Pass and Bandpass, but also includes the ability to adjust the quality factor and resonant frequency with the aid of the applied digital control. The performance has revealed a significant alteration of the transfer function for the bi-quadratic multi-functional filter responses, discussed.

These equations illustrate the transfer response for Digital Programmable Band Pass, Low Pass, and High Pass filters, respectively. The altered expressions for Excellence Factor F_Q and Resonant Angular Frequency (R_{AF}) are as follows:

$$F_Q = \frac{1}{RE_1+RE_2}\sqrt{\frac{C_1RE_1RE_2}{C_2}}$$

$$R_{AF} = \sqrt{\frac{RE_1RE_2}{C_1C_2}}$$

A. Neural Network Process

Using a back-propagation algorithm, the data patterns are used to adjust the network's weights and threshold values, which helps reduce the chances of making a wrong prediction. The simulation creates the data, and then the neural network is used to train it off-line using the back-propagation algorithm. You can use the back-propagation algorithm to train the neural network in the following steps: The error derivative is a measure of the difference between the actual and desired activity. The error derivative is calculated by multiplying the rate at which a unit's output changes as a function of its total input and computing the resulting quantity. The values are then multiplied by the unit activity level from which the connection originates as expressed. Subsequently, the mass of the connection to the output unit is multiplied by the result of the previous calculation. We use the above process to get repeated values for as many layers as we want. Once we know the values, we can compute them on the incoming connections. Using the algorithm, the digital circuit's neural network trains and validates the response based on the user-defined information.

B. Artificial Neural Network Based Logic Circuit

This model is designed to verify the BMDM (Bipolar Multidimensional Model) and Double Diffused Multidimensional Model to be decoded. It is composed of a combinational logic circuit, as illustrated in Figure 4. Artificial neural network models for BMDMs to be decoded are created by combining various logic gates, such as AND/OR/NOT/XOR/XNOR. Each logic gate is trained for its input-output data patterns through Neural-Network, and the training parameters, such as the number of generations or iterations, are presented. The model is trained until either the desired goal is reached or the maximum number of iterations are reached, whichever occurs first.

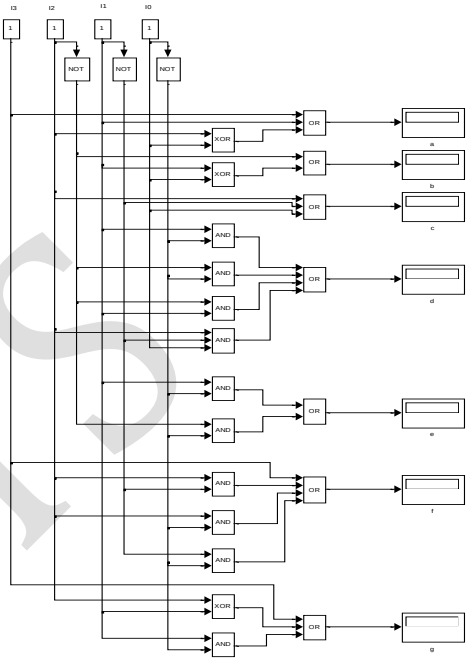

Figure.4 Logic Circuit

V-RESULT AND DISCUSSION

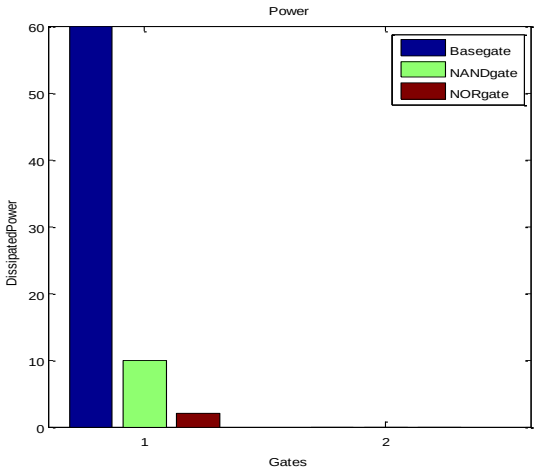

Figure 5.1 Gates Vs Power

Dissipated Power			
Gates	Base Gate	NAND Gate	NOR Gate
1	60.45	10.4756	2.35

Table 5.1 Dissipated Power

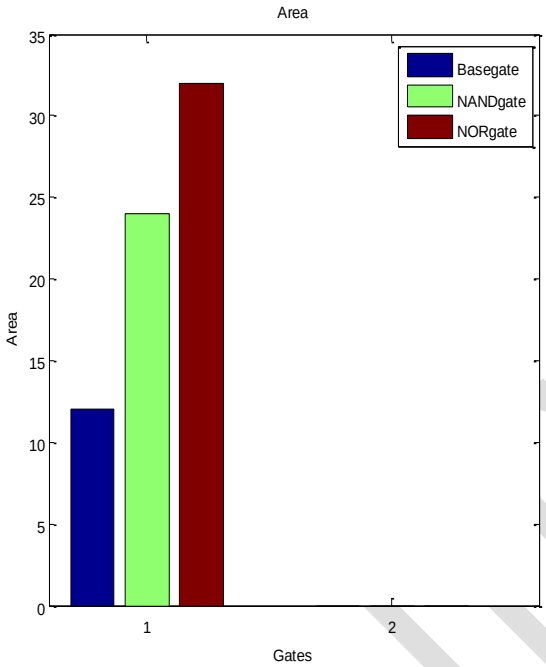

Figure 5.2 Gates Vs Area

Area			
Gates	Base Gate	NAND Gate	NOR Gate
1	12.547	24.857	32.856

Table 5.2 Area

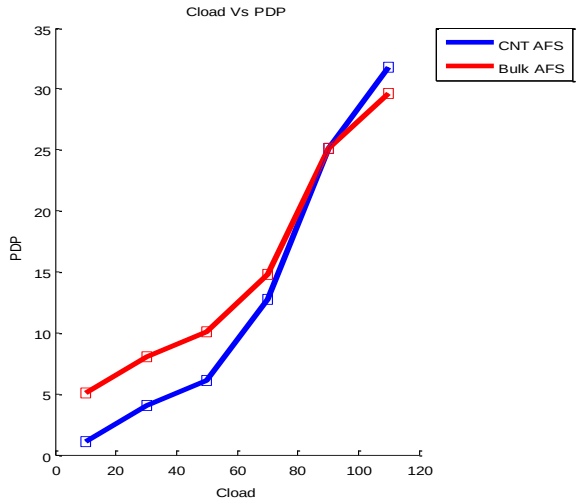

Figure 5.3 Cload Vs PDP

PDP		
Cload	CNTAFS	BulkAFS
10	1.03	5.24
30	4.023	8.322
50	6.0456	10.0395
70	12.777	14.466
90	25.0978	25.0978
110	31.7879	29.6324

Table 5.3 PDP

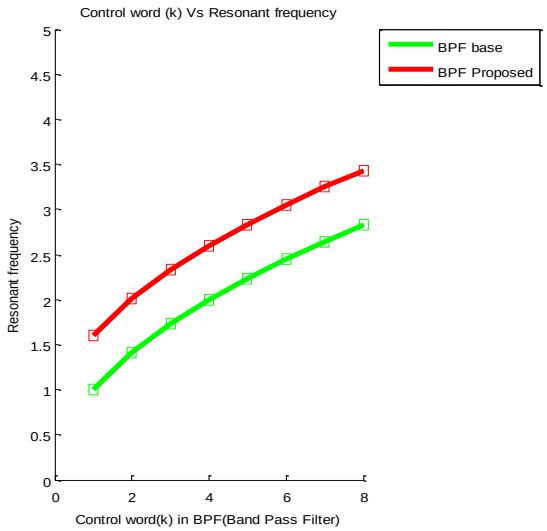

Figure 5.4 Control work(k) Vs Resonant Frequency

Resonant Frequency		
Control word(k)	BPF Base	BPF Proposed
1	1	1.60
2	1.414	2.014
3	1.732	2.332
4	2	2.60
5	2.236	2.836
6	2.449	3.049
7	2.646	3.246
8	2.828	3.428

Table 5.4 Resonant Frequency

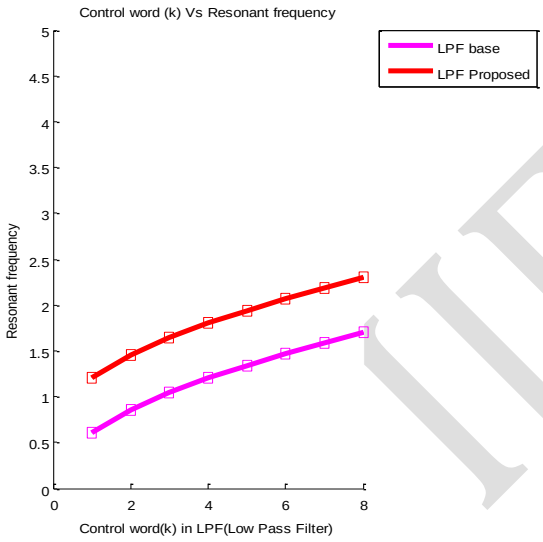

Figure 5.5 Control work(k) Vs Resonant Frequency

Resonant Frequency		
Control word(k)	LPF Base	LPF Proposed
1	0.60	1.20
2	0.849	1.449
3	1.039	1.639
4	1.20	1.80
5	1.342	1.942
6	1.470	2.070
7	1.587	2.187
8	1.697	2.297

Table 5.5 Resonant Frequency

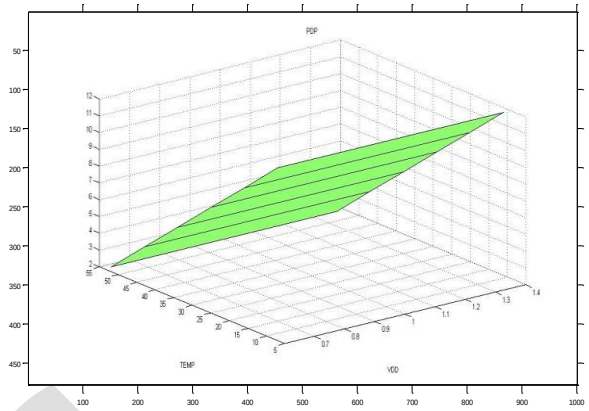

Figure 5.6 VDD Vs PDP

PDP 3D		
VDD	PDP	
0.7	2	5
0.8	3	10
0.9	4	15
1	5	20
1.1	6	25
1.2	8	30
1.3	10	35
1.4	12	40

Table 5.6 PDP

VI-CONCLUSION

In conclusion, the utilization of back propagation-based techniques in the context of Carbon Nanotube Field-Effect Transistors (CNTFETs) presents a promising avenue for achieving dynamic gate modulation and optimization. By combining the principles of machine learning with the unique characteristics of CNTFETs, researchers have demonstrated the potential to dynamically adjust gate voltages in response to varying input signals, enabling real-time optimization of transistor behavior. This innovation aligns with the growing demand for adaptable and energy-efficient electronics. Looking ahead, several

future needs and directions emerge: Developing more sophisticated algorithms that consider the complex interplay between CNTFET parameters, device physics, and dynamic input signals will enhance the accuracy and effectiveness of backpropagation-based modulation. The successful deployment of backpropagation-based gate modulation in practical devices requires extensive validation, testing, and integration into existing electronic systems to assess its robustness and reliability. Exploring multi-objective optimization techniques to simultaneously address performance metrics such as speed, energy efficiency, and reliability will enable a more comprehensive approach to transistor modulation. Investigating strategies to adapt backpropagation-based modulation to account for variability in CNT properties and manufacturing processes will be essential to ensure consistent and reliable operation. Integrating energy-awareness into the training process itself, considering the energy consumption of the neural network and its impact on overall system efficiency, can lead to more holistic optimization. Collaborations between hardware designers and machine learning experts will facilitate the development of specialized hardware accelerators and optimized neural network architectures tailored for CNTFET-based modulation. Exploring hybrid device architectures that combine CNTFETs with other emerging technologies, such as memristors or neuromorphic components, can lead to novel paradigms for adaptive and energy-efficient circuits. Developing closed-loop feedback mechanisms that enable the neural network to continuously learn and adapt based on the actual transistor behaviour will enhance the adaptability and efficiency of the modulation technique. Establishing benchmarks and standard evaluation criteria for back propagation-based CNTFET modulation will facilitate comparisons, encourage innovation, and ensure consistent performance measurement. In summary, the integration of back propagation-based techniques into CNTFET modulation holds the promise of revolutionizing transistor optimization in real-time. However, addressing technical challenges, validating its effectiveness across diverse applications, and continually refining the approach are imperative to fully harness its potential and drive the future of adaptable and energy-efficient electronics.

REFERENCE

[1] Saurabh J Shewale and Sonal A Shirsath, “Design and Analysis of CMOS Full Adder”, International Journal of Advanced Research in Science, Communication and Technology (IJARSCT), Volume 9, Issue 1, September 2021.

[2] M. Ahmadi, J. F. Webb, Z. Johari, and R. Ismail, “Single Wall Carbon Nanotube Field Effect Transistor Model”, Journal of Computational and Theoretical Nanoscience, vol. 8, no. 2, 2011.

[3] Wu J, Shen Y, Reinhardt K, Szu H, Dong B. A, “Nanotechnology Enhancement to Moore's Law. Applied Computational Intelligence and Soft Computing”, doi:10.1155/2013/426962, 2013.

[4] Navi K, Rashtian M, Khatir A, Keshavarzian P, Hashemipour O, “High Speed Capacitor-Inverter Based Carbon Nanotube Full Adder”, 2010.

[5] Gupta, S. and Arora, T.S., “Novel Current Mode Universal Filter using Single DVCC”, International Conference on Signal Processing and Communication (ICSC), 2016.

[6] Mrs. K. Srilakshmi, Naziya Parveen, K. Mahesh, L. Uday Sree and K. Durgendra Kumar, “Design and Analysis of Ultra Low Power Approximate Adder”, International Research Journal of Modernization in Engineering Technology and Science, Volume:05, Issue:04, April-2023.

[7] Dixit, A. and Gupta, N., “A Compact Model of Gate Capacitance in Ballistic Gate-all-around Carbon Nanotube Field Effect Transistors”, International Journal of Engineering, doi: 10.5829/IJE.2021.34.07A.16., Vol. 34, No. 7, 2021.

[8] Dr. S. Yuvaraj, Ph. D, Dr. K.K. Senthilkumar, Ph. D, Name Dr. K. Senthamil Selvan, Ph. D., A.R. Aravind.,M.E., “High Performance Ripple Carry Adders in VLSI Design”, International Journal of Creative Research Thoughts (IJCRT), Volume 10, Issue 6, June 2022.

[12] Imran, A., Arora, D. and Kumar, R., “Versatile Digitally Reconfigurable Current-mode Multifunctional Biquadratic Filter and Quadrature Oscillator”, Journal of Active & Passive Electronic Devices, Vol. 12, 2017.

[10] M. H. Ghadiry, A. K. A’Ain, and M. N. Senejani, “Design and Analysis of a Novel Low PDP Full Adder Cell”, Journal of Circuits, Systems, and Computers, Vol. 20, 2011.

[11] Khatir A, Abdolahzadegan SH, Mahmoudi I, “High Speed Multiple Valued Logic Full Adder Using Carbon Nano Tube Field Effect Transistor”, International Journal

of VLSI design & Communication Systems (VLSICS), 2011.

[12] K. Navi, R. S. Rad, M. H. Moaiyeri, and A. Momeni, "A Low-Loltage and Energy-Efficient Full Adder Cell based on Carbon Nanotube Technology", 2010.

[13] M. Nadi, M. H. Ghadiry, and M. K. Dermany, "The Effect of Number of Virtual Channel on NOC EDP", Journal of Applied Mathematics & Informatics, 2010.

[14] Divya Kiran Xalxo and Hitanshu Saluja, "Performance Analysis of Various Digital Adders - A Review", International Journal of Advanced Research in Science, Communication and Technology (IJARSCT), Volume 8, Issue 1, August 2021.

[15] K. Navi, M. Rashtian, A. Khatir, P. Keshavarzian, and O. Hashemipour, "High Speed Capacitor-Inverter based Carbon Nanotube Full Adder", vol. 5, no. 5, 2010.

[16] Ghorbani A, Sarkhosh M, Fayyazi E, Mahmoudi N, Keshavarzian P.A, "Novel Full Adder Cell Based On Carbon Nanotube Field Effect Transistor", International Journal of VLSI design & Communication Systems (VLSICS), 2012.

[17] Ghabri, H., Issa, D.B. and Samet, H., "Performance Optimization of 1-bit Full Adder Cell based on CNTFET Transistor", Engineering, Technology & Applied Science Research, Vol. 9, No. 6, 2019.

[18] Navi K, Sharifi Rad R, Moaiyeri M H, Momeni A., "A Low-Voltage and Energy-efficient Full Adder Cell Based on Carbon Nanotube Technology", 2010.

[19] Jain, M. and Bharti, R., "Simulation of Low Power DVCC based LNA for Wireless Receiver", IEEE, 2021.

[20] M S S M Basir, R C Ismail, S Z M Naziri , M N M Isa, S A Z Murad, and A Harun, "Speed and Area Efficient FXP Adders and Multipliers: A Comparative Analysis for LNS System", International Conference on Science, Engineering and Technology(ICSET), 2020.