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Design and Verification of Bridge Protocol to Achieve Rapid Data Synchronization between AHB and APB

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Abstract—
A Bridge is a crucial part of the design. It connects the buses on more than one clock domains. The principle element of the bridge is to transfer the data from lower buses to higher buses without losing any data synchronization. In particular this paper gives the method to design a bridge in between the high performance bus like AHB and a low performance bus like APB based on multiple methods of clock domain crossing.
Keywords—AHB, AFIFO, APB, CDC, ARM.

INTRODUCTION

A Bridge is the circuit connects busses on multi-clock domains to transfer data. Due to transferring data form a higher clock bus to lower clock bus like AHB to APB under the normal operation various problems arise, such as loss of data, metastability caused due to setup and hold violations and few troubles confronted at the same time as to synchronize among a serial and parallel architected buses .for this reason there is a need to expand a rtl circuit with a purpose to assist to synchronize these busses such that there's no problems at any stage of transferring the data.To make this synchronizing circuit, we use the clock domain crossing principles.

I. CLOCK DOMAIN CROSSING (CDC)

CDC is the methodology used for a multi-asynchronous clock designs.it considered as the heart of the bridge it helps in receiving the data from AHB Slave and transferring it to the APB master by controlling all possible issues that might arise while sending the data from one clock to another clock. Transferring a data in-between various clock domain it is called Clock Domain Crossing. Here transferring the data from AHB Slave to APB Master using principles of CDC. A data clock domains crossing mainly faces the two major problems are loss of data, metastability.

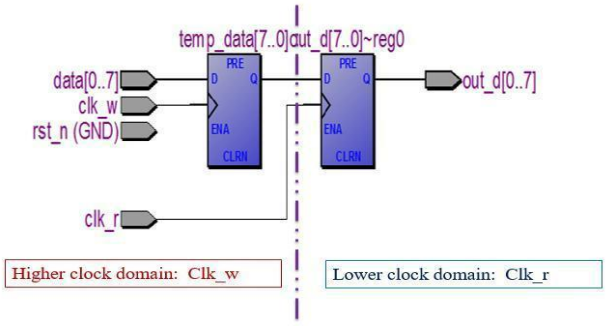
A. Loss of data

A data transfer can be done in two ways in a situation of CDC. They are firstly writing from a lower frequency to higher frequency, secondly writing from high frequency to low frequency. Generally data is transfer from low frequency domain to high frequency domain there is no loss of data ,so sampled of data will be more, but if transfer of data from high domain to a low domain loss of data will be there. So the rate of sampling for write is more than read. Hence loss of data is unpredictable. The figure.1shows the data transfer is directly between high clock and lower clock in the loss of data as shown in simulation result of figure1 and 2.

B. Metastability

Metastability indicates the values are not expect stable 0 or 1 states for some time period at the point during basic function of the design. In multiple-clock domain, metastability cannot be terminated but the issues of metastability can be grounded. The unknown output value obtained due to the setup and hold time violation of the design is called as Metastability. Metastability cannot be avoided but the results can be eliminated by using different techniques. Why the metastability is a problem? The output of the

metastable that traverses the logic additional in the receiving clock domain can illegal signal values to be propagated the entire design. Hence the CDC signal can trigger for certain time period the input logic in the accepting clock domain might recognize the logic level of triggering signal to be various ranges. In this design each flip flop is used as a particular setup and hold time in which the input data is not legally accepted to change the in and out of the rising edge of the clock. This design is specified as the part of the signal data from one to another signal synchronizing that causes the metastable to go to the output.



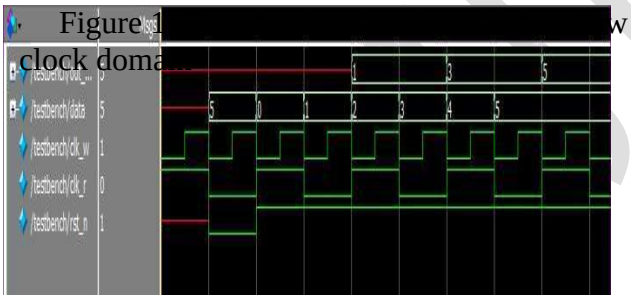


Figure 1 ...w clock doma...

Figure 2. Simulation result: Data loss

II. SOLVING ISSUES ARISED WHILE CDC

There are many methods available to solve the problems of CDC with loss of data and metastability occurred. The methods are used in this design are an AFIFO to write and read the data and by using synchronize to synchronizers the clocks sampling time without getting metastable outputs, also a gray counter is used for high speed performance and low power utilization.

A. Asynchronous FIFO

An AFIFO is placed between two modules working at various clocks domains for data_in (write or store) and data out (read or load) conditions. Let's consider the data in operation at high clock domain and data_out operation at lower clock domain. To avoid loss of data, when some part of data has to be transmitted from one module to another module. AFIFO is required only when data read is slow and write is fast. The size of the AFIFO should be maintain, all the data's are stores in FIFO. Incorporation of this structure to stores the data before it's sampled by the clock, the loss of data will be prevented in this design. To calculate the boundary by using the SIZE and BURST.In the Figure2,AHB represents HCLK, APB represents PCLK. Data in and data out operation it depends upon the clocks which resets the output, mainly depends on HCLK.

Figure 3. Asynchronous FIFO-Memory

B. Neutralize Metastability by using Synchronize Techniques:

There are two synchronization scenarios (1)It is allowed to miss tests that are passed between clocks.(2) Each values passed between clock domain may be inspected. It is important to calculate the Mean Time before Failure (MTBF) deal with metastability, always they higher values are favoured instead of lower values. Higher MTBF represents the periods of time between errors, lower MTBF represents that

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metastability could happen frequently, sampling at clock frequency (fclk) and the data change frequency (fdata) and other factor(X).AFIFO which still obeys the requirement in the circuit for an exact.design if data faces the metastability. In the design if we have any combinational settlings this will avoids those.

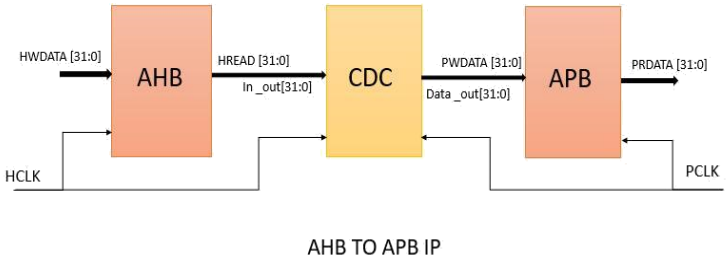
$$MTBF = \frac{1}{fclk * fdata * X}$$

C. Gray Counter

A Gray counter is preferred instead of binary counter for the placement of pointers in the AFIFO, a Gray counter for as a result of mainly two factors such as 1.change of 1- Bit in the Gray counter will reduces the event of metastability which is caused because of the combinational settling, this would affect despicable settlement of write and read pointers in the memory location. 2. A low power utilization and speed is faster in a productive design.

Inefficiency of Binary counter: In a binary counting sequence for every change in count numbers number of bits changes are more than one. This happens because the binary counter is synthesized as a ripple counter and in which carry is generated and carried along as long as it gets to the last bit of sum. This may work for binary counter, however when number of bits increment the time taken to process data is increased and there might be a possibility of combinational settling. Efficient less makes the binary counter. The next method, if the pointers are deals the combinational setting, as in the afifo have to change the address they are pointing to for any read or write instruction, they will point out the undefined address of the pointer. So it will makes the whole design to hurl. Thus the description above indicates how utilizing the binary counter impacts the design. But when a gray counter is utilized we maintain a safe distance from these problems.

Binary to Gray conversion for 4 bit binary number:



AHB TO APB IP

Figure 4. Synthesized Binary counter for transferred carry

$$gray[0] = bin[0] \; xor \; bin[1]$$
$$gray[1] = bin[1] \; xor \; bin[2]$$
$$gray[2] = bin[2] \; xor \; bin[3]$$
$$gray[3] = bin[3] \; xor \; 1'b0$$

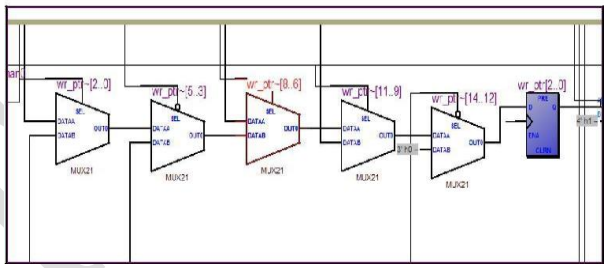


Figure 5. Preview of Entire Module

III. AHB SLAVE, INTEGRATING MULTIPLECLOCK DESIGN APB MASTER TO DESIGN A COMPLETE BRIDGE

Mainly the bridge having three parts AHB, CDC and APB. After designed the CDC part, we include an AHB as the AHB slave and an APB as an APB Master. Finally designing AHB Slave and APB Master as per the conventions given by the ARMs AMBA. Then are stitched together as shown in Figure 5 as one single AHB to APB IP. The Figure 8 demonstrates the view of the whole bridge design in the synthesis view (using Questa Sim). The information in the figure shows the data is collected by the AHB Slave for AHB Master. Then the data is stored into the memory of AFIFO as for HCLK and HWDATA and stacked from AFIFO as for PCLK and PRDATA or vice versa.

AHB Slave

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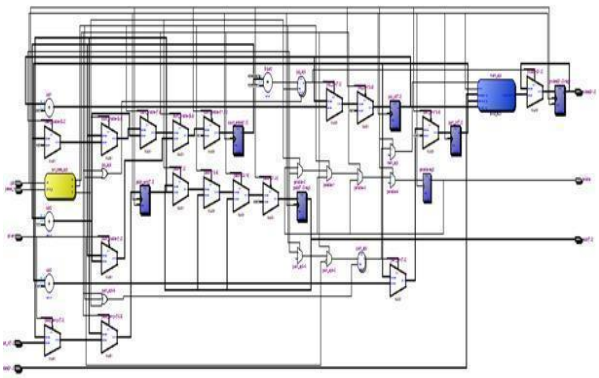
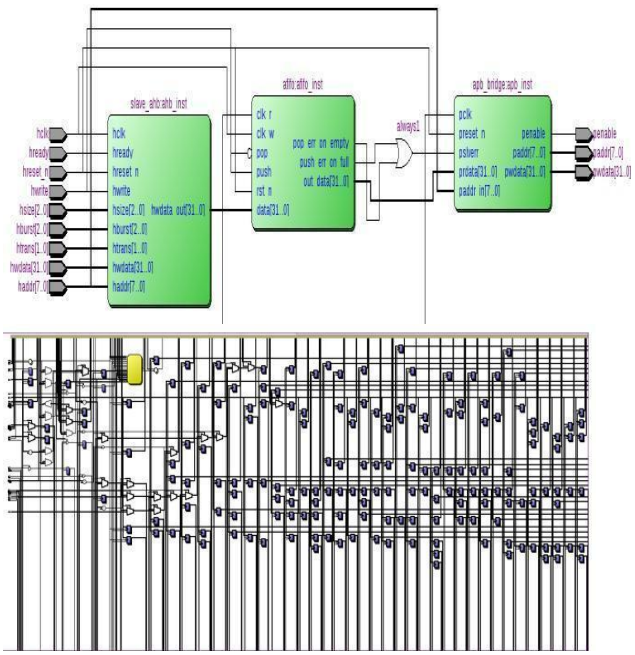
AHB (Advanced High-performance Bus), working at higher clock domain is an Advance Microcontroller Bus Architecture. It is a synthesizable design provided by ARM which is used to communicate between processors, memories such as Cache, RAM, ROM and DMA etc. in a SOC (System on Chip). AHB Architecture itself can be subdivided into two parts AHB Master and AHB Slave. The Master fetches the information from processor decodes the information and sends data to the respective the Slave. Slave further transfers to the APB Master through methodology called as Clock Domain Crossing.





APB MASTER

APB (Advance Peripheral Bus, working at lower clock domain) is an Advance Microcontroller Bus Architecture. It is a synthesizable design provided by ARM which transfers data to peripheral devices or form peripheral devices. APB Architecture can be subdivided into two parts AB Master and APB Slave. APB Master receives the information form the multiple clock design (CDC) and transfers it to APB Slave.

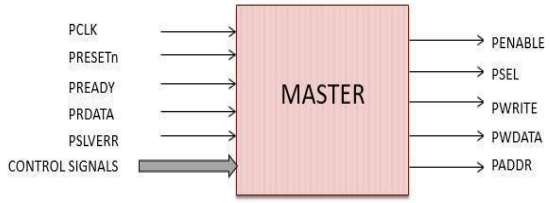
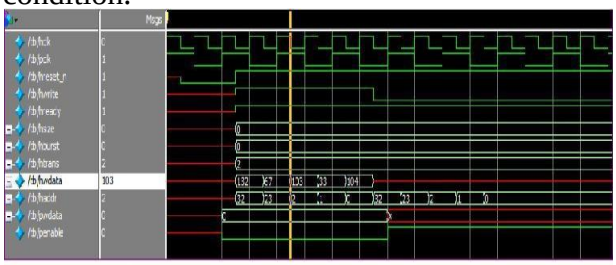
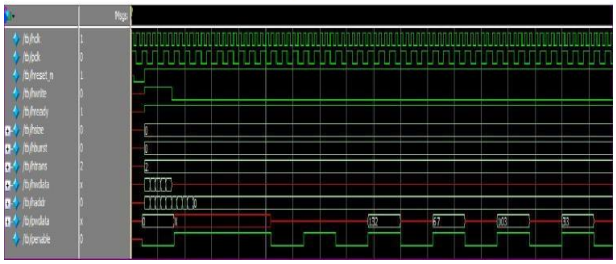


Figure 7. Block diagram of APB Master

V. THE DESIGNED BRIDGE RESULT

In the designed bridge synthesis result the HDLsimulation, timing graphs, waveforms infigures 8,9,10,11,12,13 respectively. The HDL shows has been developed using advanced Questa Sim. Simulation and synthesis results of Multi-clock Domain FIFO include with Clock domain crossing techniques in the result we can predict that there is no metastability and loss of data, thus the design is accurately in working condition.





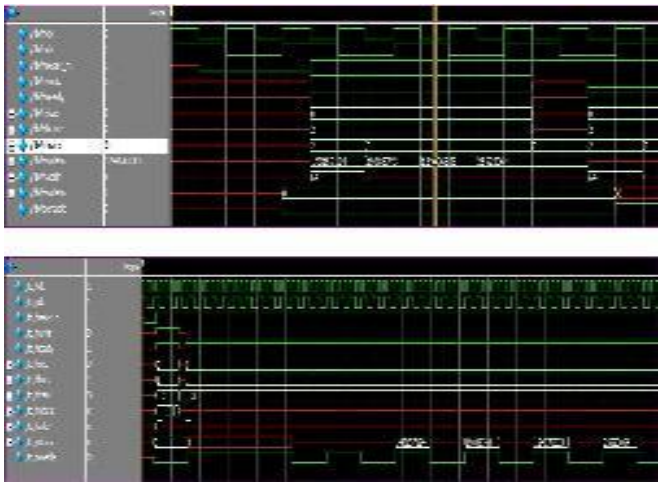


Figure 12. Simulation results of Write and Read transfers

There are distinctive transfer methods in the AHB convention which are utilized in the light kind of protocol is sent by the device. The distinctive types of transfer are transfer in single time, incremental transfer ,they are increment, increment four, increment eight, increment sixteen and wrap transfer are warp four, wrap eight, wrap sixteen. BURST signal are selected by using these signals. And built up a productive bridge design to transfer data from AHB high clock domain bus to APB low clock domain bus ,because the period of time for high clock must be at three by fourth or less than that of the period of time for low clock for ideal working.

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