CONCEPTUAL MODEL DESIGN FOR MEASUREMENT OF PRECIPITATION USING AIR BORNE RADAR

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Abstract: The development of Radar for an earth observing satellite system for global measurement of precipitation is issue of high performance. Dual frequency (14 and 35 GHz) precipitation radar is designed using EPGA as DSP technology would not handle around 40 billion op/s in few chips. Performance parameters such as swath width, spatial resolution and precision should be improved with low earth orbiting rainfall radar. In this paper, we will present onboard processor design with 40 x 10^9 op/sec and sidelobe performance of 72 dB of rainfall radar. FPGA have capability of million gate densities supporting this rate of processing.

Key terms – Global precipitation Measurement (GPM), field programmable gate arrays (FPGAs), pulse compression, space borne radar, Dual frequency Precipitation Radar (DPR).

I. Introduction

For rainfall detection, the spatial resolution, swath width and precision of measurements will be needed using an earth-orbiting space-borne radar. Dual-frequency precipitation Radar (DPR) is being developed as part of Global precipitation Measurement (GPM) mission. DPR with one KU-band radar & one Ka-band inherits phased array antenna. The key features of a low earth orbiting DPR is that it can recover the vertical profile and structure of precipitation to infer how liquid water and latent heat are transported in the atmosphere[1]. DPR consist of vertical structure of rain reflectivity at both copolarization and cross-polarization at frequencies 13.6 GHz and 35 GHz.

With spacecraft altitude 400 km, DPR scans its dual-frequency antenna beams having downward looking radar. DPR is designed using a chirp radar techniques. Chirp pulse width of 50 us gives a vertical range resolution of 250 m which is quite large compared to short pulse radar system.

The electronics subsystem consists of chirp generator used to synthesize a linear frequency-modulated chirp waveform, T/R modules for dual-frequency beam and upconverters and downconverters for a receive channels. The chirp waveform is generated at an IF frequency and upconverted to both 14 and 35 GHz. The signals are then amplified using linear tower amplifier in T/R modules and then sent to the dual frequency feeds and antenna. There are four receiver channels – two for 14 GHz, (H- and V- pol) and two for 35 GHz, (H- and V- pol) [2][3].

This project involves the development of a high-performance onboard digital data processor and timing unit implemented in field-programmable gate arrays (FPGA). Adaptive scanning makes it possible to collect 3-D rainfall profiles with swath width of 500 km.

In this paper, we will describe the development of onboard processor/controller system. The design of our FPGA based data processor for pulse compression and averaging of the received radar echoes is described in following section.

II. Pulse compression processor

Pulse compression originated with the desire to amplify the transmitted impulse power by temporal compression. It combines the high energy of long pulse width with the high resolution of a short pulse width.
Fig. 1 Data Compression

Ability of the receiver to improve the range resolution is

\[ \text{PCR} = \frac{C_0 \cdot T}{2} / B \cdot T \]

\[ R_{\text{res}} = \frac{C_0 \cdot (T/2)}{3B} \cdot \text{PCR} = \frac{C_0}{2B} \]

For time-domain pulse compression using matched F/R filter banks, the number of complex filter coefficients is driven by the 200-fold compression ratio. The choice of windows becomes a tradeoff between range resolution and range side lobe levels. Our design shows that an optimal trade could be met by using Kaiser window resulting in 3-DB range width of 470 ns for 50 μs chirp pulse.[9]

Processing rate of DPR is 256 filter taps x 5 MHz baseband x 1 real filter x 2 maths ops. x 1 radar channel = 10.96 x 10^9 op/s.

DSP would not be a practical choice meeting 10 billion op/s per channel (since 4 channels are there) as a large no. of processing cheks would be needed on board. As an alternative, FPGA and makes it possible to support this processing rate.

III. Data processor design

The signal chain for data processor is illustrated in fig. The onboard processor is designed with FIR filter.

Data enter the RPGA and as four channels of 12 bit data at 20 MHz sampling rate. The 4 MHz chirp data are centered around a 5 MHz carrier.

The first stage consist of demodulator which translated the 20 MHz samples into 5 MHz baseband data. Demodulator consists of a mixer, low-pass antialiasing filter and a decimator which reduces output data rate by a factor of 4. A 64-tap, 16-bit FIR filter is excluded in hardware implementation.

The 5 MHz complex baseband are stored in a first in / first our memory so the echoes containing saturated samples are detected and eliminated before range compression.

A lowpass anti-aliasing filter, and a decimator which reduces the output data rate by a factor of 4. There is no loss of information in the decimate-by-4 operation, given that the signal of interest is limited to < 5 MHz bandwidth and that aliased frequency components have been removed. The actual implementation of the complex demodulator is made with a polyphase demodulator, which combines the mixing, filtering and decimation operations in one stage [9]. A 64 tap, 16-bit polyphase FIR filter is included in the digital hardware implementation of this demodulator.

The 5 MHz complex baseband data is stored in a first-in/first-out memory so that pulses containing saturated samples can be eliminated. Data is then fed into a 256-tap, non-symmetric FIR filter which contains the complex conjugate of the expected return. This is where the bulk of the FPGA’s processing resources are used, amounting to 20 billion real multiply and add operations per second. The output of this 256-tap filter is the compressed radar return. Complex data is converted to power and averaged over adjacent range bins and multiple pulses. Averaging provides two orders of magnitude data compression. Further range averaging is applied for adaptive scanning, described in the next section, to identify the beams most likely to contain rain.
A number of digital signal processing (DSP) applications make this processing density possible. Bit-serial filtering makes best use of the speed capabilities of the FPGA. The FIR filter stage uses a lookup table to combine 4 stages of multiplication and addition into a single configurable logic block. The video filter, demodulator, and downsampler are actually four parallel filter stages which compute only the samples which are kept after decimation. Complex-valued filtering is implemented by running delay stages and multipliers at double speed and switching between real and imaginary components of each received waveform, saving half of the FPGA.

IV. CONTROL AND TIMING UNIT (CTU)
A unique feature of precipitation is that it is often sparsely distributed over the Earth's surface. Even for weather in tropical regions, which accounts for more than half of the total global rainfall, precipitation occurs over only 4% of the surface area [5]. This statistic can be exploited in the DPR by using an adaptive scanning technique [10]—that is, the radar can use its own preliminary "quick-scan" data to electronically steer the radar beam to only those areas which contain precipitation, and to ignore areas that are precipitation-free. With adaptive scanning, the dwell time for the rain target can be increased 7 times beyond that of a conventional cross-track scanning radar without sacrificing swath width.

We have developed a specialized Control and Timing Unit (CTU) with an adaptive scanning algorithm onto FPGA. This CTU generates the transmit and receive timing for an entire 300 ms sweep cycle, consisting of: 1) a locator sweep that performs a rough measurement of echo return power over all cross-track beam locations (248 beams) and over an 8 km altitude range; 2) a bubble-sort algorithm which ranks the 248 beam locations from highest to lowest return powers; and 3) a high-resolution sweep, which takes additional radar looks of the top 24 ranked beams over a longer 12 km altitude range. The timing solution for the CTU must be generated on-the-fly with minimum dead-time between echoes-in-flight (EIFs), while also avoiding collisions between transmit and receive echoes.

Because of the critical timing constraints of the adaptive scan, we chose to implement the CTU with a network of custom-made state machines in the FPGA rather than with a microprocessor core. The advantage to using state machines is that they can respond immediately and in-parallel to a large number of timing interrupts. Fig. 2 shows a diagram of the key logic modules developed for the CTU.

The sweep engine module includes an EIF counter array which keeps track of the location of up to 32 radar echoes and provides feedback to guarantee that transmit and receive pulses are interlaced. A bubble-sort machine takes echo return values from the locator sweep and executes a sorting algorithm of order $O(N^2)$ in the block RAM of the FPGA. An antenna driver module then sends
beam steering data from an SRAM lookup table to 2,300 phase-shifters in the PR-2’s antenna array to define the present locations of transmit and receive beams.

All of the digital circuitry for the CTU has been designed at the register transfer level using the Verilog hardware description language. The CTU design currently uses ~1900 flip flop storage elements and ~79000 logic gates[11] which are interconnected in an array of Virtex configurable logic blocks. To guarantee that setup and hold timing requirements are met between registers, we implemented the CTU logic as a synchronous design (with all registers tied to a common 20 MHz clock) and ran it through a static timing analysis. Fig. 3-

**Fig.3** Illustration of steps involved in the adaptive scanning sequence.

V. ADAPTIVELY SCANNING

A unique feature of precipitation is that it is often sparsely distributed over the earth’s surface. Even for weather in tropical regions, which accounts for more than half of the total global rainfall, precipitation occurs over only 4% of the surface area [7]. This statistic can be exploited in the DPR by using an adaptive scanning technique that is, the radar can use preliminary "quick-scan" data to electronically steer the radar beam to only those areas which contain precipitation, and to ignore areas that are precipitation-free.

Adaptive scanning becomes all the more necessary as the observation requirements for future spaceborne rainfall measuring missions move toward higher horizontal resolution and larger swath widths—the two opposing requirements that compete against the available dwell time. Compared to TRMM’s PR observations or to the DPR observations planned for the GPM mission, the DPR represents a 12-fold increase in the number of radar beam positions per swath area (a six-fold increase due to horizontal resolution improvements in two dimensions and a two-fold increase in swath width). Given the limited dwell time of a 7-km/s low-earth orbiting satellite, the timing sequence for interlacing the transmit and receive beams becomes critical. The radar must be able, in real time, to selectively dwell on only those beam locations that have rainfall and then generate a transmit/receive timing solution that can capture 60 or more independent radar looks needed [6] to accurately estimate the reflectivity of each rain bin. Conventional cross-track scanning radars, such as the TRMM PR, scan in a predetermined, right-to-left sequence at a constant pulse repetition frequency (PRF). However, a constant PRF scanning method does not make the most efficient use of the satellite's available dwell time over the rain target, due to the resultant "dead time" or gaps between the transmitted and received pulses. A more intricate transmit and receive timing scheme with variable PRF has been proposed for the GPM DPR design to increase the number of radar looks within the cross-track sweep period as the beam is steered inclusively,

**TABLE- DPR PARAMETERS[5]**
from right to left [10]. This scheme does not accommodate adaptive scanning, though, of the same rain bin are statistically independent. Second, the adjacent beam sequence ensures that each series of pulses has essentially the same round-trip range delay time (and therefore equal PRF over each beam position pair) so that Rule 2 is never violated.

VI. Conclusion

We have presented an overview of Dual Frequency Precipitation Radar’s on-board digital electronics design, which includes a pulse compression processor with very low range sidelobe performance and a new adaptive scanning controller. The on-board processor /controller will serve as a key subsystem for a future satellite precipitation mission having dual frequency (13 and 36 GHz) capabilities.

REFERENCES


